VERIFICATION OF TRANSLATION

I, ITOME Shigeki, a citizen of Japan, currently residing at #201 4-19-3 Senrioka-Higashi Setsu-Shi, Osaka, Japan, hereby declare:

That I am fully familiar with the English language and with the Japanese language in which the accompanying Japanese Language Application No. 2002-218779 was prepared;

That the annexed English text is believed by me to be a true and accurate translation of the text of said Japanese Language Application; and

That all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed at <u>Osaka, Japan</u>
Date: <u>February 20, 2007</u>

Signature: _____
ITOME Shigeki

日 本 国 特 許 庁
JAPAN PATENT OFFICE

　別紙添付の書類に記載されている事項は下記の出願書類に記載されている事項と同一であることを証明する。

　This is to certify that the annexed is a true copy of the following application as filed with this Office

出 願 年 月 日
Date of Application:　　　２００２年　７月２６日

出 願 番 号
Application Number:　　　特願２００２−２１８７７９

[ST.10/C]:　　　　　　　[ＪＰ２００２−２１８７７９]
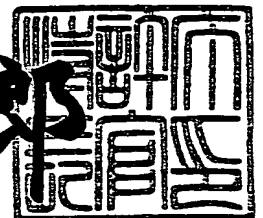
出 願 人
Applicant(s):　　　シャープ株式会社

２００３年　６月１７日

特 許 庁 長 官
Commissioner,
Japan Patent Office　　　太田信一郎

[DOCUMENT NAME] SPECIFICATION

[TITLE OF THE INVENTION] CORRELATOR

[CLAIMS]

[Claim 1]

A correlator which figures out a correlation between an input signal which is an inpulse train and a predetermined time-series signal, characterised by comprising:

a multiplier for multiplying the input signal by the predetermined time-series signal;

an integrator for integrating an output (i) from the multiplier;

a quantizer for quantizing an output (ii) from the integrator; and

a negative feedback path from an output (iii) of the quantizer back to an input of the integrator.

[Claim 2]

A correlator which figures out a correlation between an input signal which is a pulse train and a predetermined time-series signal, characterised by comprising:

a multiplier for multiplying the input signal by the predetermined time-series signal;

a first integrator for integrating an output (a) from the multiplier;

a sampling circuit for sampling an output (b) from the first integrator;

a second integrator for integrating an output (c) from the sampling circuit;

a quantizer for quantizing an output (d) from the second integrator; and

a negative feedback path from an output (e) of the quantizer back to an input of the second integrator.

[Claim 3]

The correlator as defined in claim 2, characterised in that, the first integrator is an integrator which attenuates at a certain time constant.

[Claim 4]

A correlator characterised by comprising a plurality of correlators as defined in any one of claims 1 to 3.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[INDUSTRIAL FIELD OF THE INVENTION]

The present invention relates to a correlator (matched filter) for examining the correlation between an input impulse train (string) and a time-series signal, and particularly relates to a correlator for UWB (Ultra Wide Band) communication.

[0002]

[PRIOR ART]

Recent explosive growth of various information-communication devices typified by mobile phones and PDAs has accelerated the shortage of available frequency bands. In the meantime, today's highly-networked information society boosts demand for multimedia mobile communications utilizing time-varying (animation) images and great amounts of data. In this background, what has been researched is impulse radio (Ultra Wide Band Radio, UWB Radio) technology which opens the way for realizing communication or instrumentation (radar) without causing interferences with conventional radio communications, by means of impulses with minimum power spectral density, which can broadly spread the spectrum (from very low frequency to GHz range) (cf. Nikkei Electronics, Published on 2002,

3,11, P. 55 - 66).

[0003]

Referring to Figs. 5 and 8, an example of this impulse radio is described below. Fig. 5 illustrates a monocycle for the impulse radio. A monocycle (unit cycle) 10 is approximated by Equation 1.

[0004]

[Equation 1]

$$S(t) = \frac{\tau}{t} exp \left(- \left(\frac{\tau}{t}\right)^2\right)$$

[0005]

In this equation, "τ" indicates a time constant for determining the width of the monocycle. In the impulse radio, communication or instrumentation is performed using a time-series signal in which a monocycle 10 where τ is typically in the range of 0.1 nanosecond to 1 nanosecond is repeated at intervals (e.g. in the range of 10 nanosecond to 1000 nanosecond) longer than τ.

[0006]

Fig. 6 illustrates an example of a template for the impulse radio. A template 20 is equivalent to the difference between two monocycles being shifted from each other for $(2^{0.5})\tau$. The cross-correlation between this template 20 and the monocycle 10 is illustrated as a graph of a correlation

30 in Fig. 6. Thus, when the monocycle 10 is received and the correlation between this monocycle 10 and the template 20 is figured out, a correlation value is: 0, provided that the timing of the monocycle 10 is in agreement with the timing of the template 20; positively maximum, provided that the monocycle is ahead of the template for $\tau/2^{0.5}$; or negatively maximum, provided that the monocycle is behind the template for $\tau/2^{0.5}$. On the basis of this principle, communication or instrumentation using an impulse train having been subjected to pulse position modulation is performed.

[0007]

Referring to Fig. 8, a method for transmitting binary data by means of impulse radio will be described. In this example, an average interval of transmitting a monocycle is T/N. For spread spectrum and channel multiplexing, the instant of transmitting the monocycle is varied using a pseudo-random code sequence. More specifically, in accordance with the value of the pseudo-random code which is either +1 or -1, it is determined whether the instant of the transmission is retarded for Δt or advanced for Δt, from an instant determined by the average transmission interval.

[0008]

To transmit sets of binary data +1 and -1 at intervals T, an impulse train SL(t) is used for the set of data +1. The impulse train SL(t) repeatedly transmits the monocycle for N times, and instants of the transmission are $\tau/2^{0.5}$ later than the above-mentioned retarded or advanced instants. When the set of binary data -1 is transmitted, an impulse train SE(t) is used. The impulse train SE(t) repeatedly transmits the monocycle for N times, and the instants of the transmission are $\tau/2^{0.5}$ earlier than the above-mentioned retarded or advanced instants. To demodulate the data in response to the receipt of the impulse train SL(t) or SE(t), a template train TP(t) is used. This template train TP(t) is a signal in which the template 20 is repeated for N times, and the templates 20 are generated at the above-mentioned retarded or advanced instants.

[0009]

A receiving device which has received the impulse train SL(t) or SE(t), figures out the correlation between the impulse train SL(t) or SE(t), and the template train TP(t). Here, it is assumed that, using an appropriate means (e.g. delay lock loop) for typical communications, the received

impulse train SL(t) or SE(t), is in sync with the template train TP(t).

When the received signal is the impulse train SL(t), a correlation value between each of the monocycles 10 and each of the templates 20 is a negative maximum value so that it is possible to obtain a negative value as a correlation value which is figured out by adding the negative maximum value for N times. In contrast, when the received signal is the impulse train SE(t), a correlation value between each of the monocycles 10 and each of the templates 20 is a positive maximum value so that it is possible to obtain a positive value as a correlation value figured out by adding the positive maximum value for N times.

[0010]

For instance, US Patent No. 5,363,108, titled "TIME DOMAIN RADIO TRANSMISSION SYSTEM" discloses a technique for communication and a radar device utilizing impulse radio. According to the block diagram in Fig. 9 illustrating a transmitter receiving device, a received signal is: in a mixer 230, multiplied by a pattern generated by a template generator 232; integrated by an analog integrator 250; and amplified by an amplifier 252.

Then the received signal is sampled by a sample and hold 254, quantized in an A/D converter 256, and finally integrated by a digital integrator 262 so that a correlation value is produced.

[0011]

[TECHNICAL PROBLEM]

However, according to the above described system, since a quantization error arises in the signal each time the A/D converter 256 carries out the quantization, a SN (Signal to Noise) ratio of the signal deteriorates. To improve the SN ratio, it is necessary to increase the quantifying bit number of the A/D converter 256. However, this significantly increases the power consumption.

[0012]

The objective of the present invention is to provide a correlator which is suitably used as a part of a receiving device for impulse radio. More specifically, the objective of the present invention is to provide a correlator which receives an impulse train and figures out a correlation between the impulse train and a predetermined time-series pattern, in the correlator a quantization error caused in the process of quantization being reduced.

[0013]

[TECHNICAL SOLUTION]

To solve this problem, a correlator in accordance with the present invention is characterized by comprising: a multiplier for multiplying an input signal by a predetermined time-series signal; an integrator for integrating an output (i) from the multiplier; a quantizer for quantizing an output (ii) from the integrator; and a negative feedback path from an output (iii) of the quantizer back to an input of the integrator.

[0014]

According to this arrangement, since the output (iii) is negatively fed back to the analog integrator, a quantization error in the output (iii), which has been arisen in the process of quantization, is negatively fed back to the analog integrator and integrated thereby, and then quantized by the quantizer again. Hence, a quantization error can be significantly decreased.

[0015]

To solve the above-mentioned problem, another correlator of the present invention is characterized by comprising: a

multiplier for multiplying an input signal by a predetermined time-series signal; a first integrator for integrating an output (a) from the multiplier; a sampling circuit for sampling an output (b) from the first integrator; a second integrator for integrating an output (c) from the sampling circuit; a quantizer for quantizing an output (d) from the second integrator; and a negative feedback path for negatively feeding an output (e) from the quantizer back to the second integrator.

[0016]

According to this arrangement, a quantization error can be significantly decreased as in the foregoing correlator of the present invention.

Further, since the first integrator requiring quick response and the second integrator having a long holding time are provided to be independent from each other, the overall power consumption of the integrators can be reduced. More specifically, the load-carrying capacity of the first integrator is reduced and as a result the power consumption thereof is reduced, while the output from the first integrator is integrated by the second integrator which operates at a low speed, uses less power, and has a long holding time. Thus, it is possible to reduce the

overall power consumption.

[0017]

Furthermore, the first integrator is preferably an integrator which attenuates at a certain time constant.According to this arrangement, when the time constant is a value which allows (i) the product of a monocycle and a template (time-series signal) to be precisely integrated, and (ii) an attenuation time constant to be sufficiently attenuated before the next monocycle, it is unnecessary to reset the first integrator.

[0018]

Furthermore, a correlator of the present invention may include a plurality of the above-mentioned correlators. With this arrangement, the correlations between the respective template trains having different phases and the input signal can be calculated in a parallel manner. This can be utilized for operations such as the acquisition and tracking of synchronization with the input signal.

[0019]

[EMBODIMENTS]

[First Embodiment]

The following will describe First Embodiment of the

present invention with reference to Fig. 1.

[0020]

Upon the input of an input signal 500 which is an impulse train from an impulse radio transmitter, a correlator 50 in accordance with the present embodiment calculates a correlation value between this input signal 500 and a template train 502, and as a digital correlation output signal 509, the correlator 50 outputs the result of the calculation. The correlator 50 includes a multiplier 501, a template generator 503, an adder 504, an analog integrator 505, a quantizer 506, and a digital integrator 508 (integrator).

[0021]

The template generator 503 generates a template train 502 (time-series signal) which is identical with a template train TP(t) in Fig. 8. This template train 503 is a signal in which a monocycle is repeated for N times. The template train 502 is, as described above, generated at the above-described instant determined by varying an average transmission interval T/N by a pseudo-random code.

[0022]

The multiplier 501 multiplies the input signal 500 by the template train 502, and outputs the result of the

multiplication. The adder 504 adds the output from the multiplier 501 to an output from the quantizer 506 and outputs the result of the addition.

[0023]

The analog integrator 505 is an analog circuit which outputs an integration value of the output from the adder 504. The quantizer 506 is a circuit which quantizes the output from the analog integrator 505, and output a digital integration value. The digital integrator 508 outputs the digital integration value, which has been supplied from the analog integrator 505, as a correlation value. The digital value from the quantizer 506 is supplied to the adder 504 via a negative feedback path 507.

[0024]

The above-described template generator 503, the quantizer 506, and the digital integrator 508 operate in accordance with the timing of a clock 510.

[0025]

Next, the operation of the above-mentioned correlator 50 will be described.

[0026]

First, the input signal 500 is represented as x(t) which is a function of a time instant t, and the template train 502

generated in the template generator 503 is represented as y(t) which is a function of a time instant t. A cycle of the template train is represented as T, an interval that the quantizer 506 quantizes the output from the analog integrator 505 is represented as ΔT, and $T/\Delta T = M$. Further, time instants at which the quantizer 506 samples and quantizes the output from the analog integrator 505 are represented as ..., T_i, T_{i+1}, ..., and provided that the output from the analog integrated 509 at the time instant T_i is represented as $f(T_i)$, the output from the quantizer 506 at the time constant T_i is represented as $q(T_i)$, and a quantization error is represented as δi, the following Equation 2 stands.

[0027]

[Equation 2]

$$f\ (T_j) = q\ (T_j) - \varepsilon_j$$

[0028]

Assuming that a start time instant of one template train is T_i and an end time instant thereof is T_{i+M}, an output $f(T_{i+M})$ from the analog integrator 505 at the time instant T_{i+M} is represented as Equation 3.

[0029]

[Equation 3]

$$f(T_{i+M}) = \int_0^{T_i} (x(t)\,y(t) - Aq(t))\,dt + \int_{T_i}^{T_i+M} (x(t)\,y(t) - Aq(t))\,dt$$

$$= f(T_i) + \int_{T_i}^{T_i+M} (x(t)\,y(t) - Aq(t))\,dt$$

$$= q(T_i) - \varepsilon_i + \int_{T_i}^{T_i+M} x(t)\,y(t)\,dt - \int_{T_i}^{T_i+M} Aq(t)\,dt$$

$$= q(T_i) - \varepsilon_i + \int_{T_i}^{T_i+M} x(t)\,y(t)\,dt - \sum_{k=i}^{i+M-1} q(T_k)\,dt \cdots$$

$$= -\varepsilon_i + \int_{T_i}^{T_i+M} x(t)\,y(t)\,dt - \sum_{k=i+1}^{i+M-1} q(T_k)\,dt$$

[0030]

In Equation 3, A indicates a gain of the negative feedback path 507, and A=N/T. In the meantime, since Equation 4 is obtained from Equation 2, substituting Equation 4 for the left side of Equation 3 results in Equation 5.

[0031]

[Equation 4]

$$f(T_{i+M}) = q(T_{i+M}) - \varepsilon_{i+M}$$

[0032]

[Equation 5]

$$\int_{T_i}^{T_i+M} x(t)y(t)dt = -\varepsilon_{i+M} + \varepsilon_i + \sum_{k=i+1}^{i+M} q(T_k)$$

[0033]

According to Equation 5, the left side which is a correlation value between the input signal $x(t)$ and the template train $y(t)$ during a period between the time instants T_i and T_{i+M} can be quantized as in the third term of the right side, and the quantization error on this occasion is given by $-\varepsilon_{i+M}+\varepsilon_i$. In reality, the digital integrator 508 performs integration when receiving an output $q(T_k)$ from the quantizer 506, and then outputs the above-mentioned value of the third term of the right side, as a value of the digital correlation output 509. Note that, if the analog integrator 505 is reset at the time instant T_i and $f(T_i)=0$ is met, the quantization error ε_i is 0, and this ensures further decrease of the quantization error.

[0034]

The reset of the analog integrator 505 is, for instance, performed by turning on a switch (not illustrated) for discharging integrated electric charges. A signal for switching on/off the switch is either periodically generated in accordance with a clock by means of a counter or generated by a CPU for controlling the receiver.

[0035]

Using the correlator 50 of the present embodiment, the

left side of Equation 4, which is the correlation value during the time instant T_i to the time instant T_{i+M} can be quantized as in the third term of the right side, and the quantization error thereof is given by either $-\varepsilon_{i+M}+\varepsilon_i$ or $-\varepsilon_{i+M}$. However, if the negative feedback path 507 illustrated in Fig. 1 is not provided, the quantization errors arisen each time the quantization is performed are accumulated for M times, during the period from the time instant T_{i+1} to the time instant T_{i+M}. Thus, when the negative feedback path 507 is provided, the SN ratio improves in proportion to the square root of M.

[0036]

[Second Embodiment]

The following will describe Second Embodiment of the present invention, with reference to Fig. 2.

[0037]

To a correlator 60 in accordance with the present embodiment, an input signal 600 which is an impulse train is supplied from an impulse radio transmitter, and the correlator 60 calculates a correlation value between this input signal and a template train 602 so as to output the result of the calculation as a digital correlation output

signal 609. The correlator 60 is arranged so as to be identical with the correlator 50, except a DA converter 607. In other words, a multiplier 601, a template generator 603, an adder 604, an analog integrator (integrator) 605, a quantizer 606, and a digital integrator 608 are equivalent to the template generator 503, adder 504, analog integrator 505, quantizer 506, and digital integrator 508, respectively. The DA converter 607 is provided on a negative feedback path 10, and converts the output supplied from the quantizer 606 to an analog signal and outputs the converted signal to the adder 604.

[0038]

The template generator 603, the quantizer 606, and the digital integrator 608 operate in accordance with the timing of a clock 610.

[0039]

In the case of the correlator 50, the quantizer 506 performs binary quantization. Thus, since a binary digital output represented as, for instance, +1 and -1 can be regarded as an analog signal, the signal can be negatively fed back to the adder 504 without any modification.

In the case of the correlator 60, the quantizer 606 may deal with 3 or more quantized values. Thus, since the

quantized output generally cannot be regarded as an analog value, the output is converted to an analog value by the DA converter 607, and then negatively fed back to the adder 604. Also in this case, the equations described in Embodiment 1 stand. For this reason, as an output from the digital integrator 608, a desirable correlation value can be obtained.

[0040]

[Embodiment 3]

The following will describe Embodiment 3 of the present invention with reference to Fig. 3.

[0041]

To a correlator 70 in accordance with the present embodiment, a signal 700 is supplied from an impulse radio transmitter. The correlator 70 calculates a correlation value between the supplied signal and a template train 702, and outputs the result of the calculation as a digital correlation value 711. The correlator 70 includes a multiplier 701, a template generator 703, a first analog integrator (first integrator) 704, a sampling switch (switching circuit) 705, an adder 706, a second analog integrator (second integrator) 707, a

quantizer 708, a negative feedback path 709, and a digital integrator 710.

[0042]

The multiplier 701 and the template generator 703 are equivalent to the above-described multiplier 501 and template generator 503, respectively.

[0043]

The first analog integrator 704 is an analog circuit which outputs integration value of the output supplied from the multiplier 701. The sampling switch 705 samples the output from the first analog integrator 704, at predetermined sampling intervals determined in accordance with a clock 712, so as to output the sampled signal.

[0044]

The adder 706 adds the output from the sampling switch 705 to the output from the quantizer 708, and outputs the result of the addition. The second analog integrator 707 is an analog circuit which outputs an integration value of the output supplied from the adder 706. The quantizer 708 is a circuit which quantizes the output from the second analog integrator 708, and outputs a digital integration value.

The digital integrator 710 outputs the digital integration value supplied from the quantizer 708, as a digital correlation value (digital correlation output signal) 711. Further, the digital value is supplied from the quantizer 708 to the adder 706 via the negative feedback path 709.

[0045]

The above-described template generator 703, sampling switch 705, adder 706, quantizer 708, and digital integrator 710 operate in accordance with the timing of the clock 712.

[0046]

Next, the operation of the above-mentioned correlator 70 will be described.

[0047]

In the present embodiment, the input signal 700 and the template train 702 are multiplied in the multiplier 701, and the resulting output is, first of all, integrated by the first analog integrator 704. The output from the analog integrator 704 is sampled by the sampling switch 705 at predetermined sampling intervals, and then supplied to the adder 706, as a discrete-time analog signal.

[0048]

Also to the adder 706, the output from the quantizer 708

is negatively fed back via the negative feedback path 709. As in the case of the DA converter 607 in the correlator 60 of Second Embodiment, the negative feedback path 709 may be replaced with a DA converter for converting the output, supplied from the quantizer 708, to an analog value.

[0049]

As a discrete-time analog value, the output from the adder 706 is integrated by the second analog integrator 707, sampled at predetermined sampling intervals in accordance with the clock 712, and then quantized by the quantizer 708. The output from the quantizer 708 is supplied to the digital integrator 710 and integrated thereby, then outputted as the digital correlation value 711.

[0050]

In the present embodiment, the first analog integrator 704 can perform attenuation. In this connection, it is preferable that a time constant of the attenuation is a value which allows (i) the product of a monocycle and a template to be precisely integrated, and (ii) the attenuation to be sufficiently performed before the next monocycle.

[0051]

Even if an integrator which does not have the above-described attenuation characteristics so that the holding time thereof is relatively long is adopted as the first analog integrator 704, it is possible to construct a desirable correlator by resetting the first analog integrator 704 after the sampling switch samples the integration value.

[0052]

Further, in the correlator 70 of the present embodiment, the first analog integrator 704 requiring quick response and the second analog integrator 707 having a long holding time can be provided to be independent from each other. As described below, this arrangement makes it possible to reduce the power consumption of the first and second analog integrators 704 and 707.

[0053]

Since a frequency band of an integrator is in inverse proportion to a load-carrying capacity, it is necessary to reduce the capacity for integration, in order to reduce the power consumption while keeping a necessary frequency band. In contrast, since a time constant of attenuation characteristics of an integrator is in inverse proportion to

an integration capacity, it is necessary to increase the integration capacity to keep a sufficient length of holding time. Concerning this, the first and second analog integrators 704 and 707 are provided to be independent from each other. Thus, the load-carrying capacity of the first analog integrator 704 is reduced and as a result the power consumption thereof is reduced, while the output from the first analog integrator 704 is integrated by the second analog integrator 707 which operates at a low speed, uses less power, and has a long holding time. Thus, it is possible to reduce the overall power consumption..

[0054]

[Fourth Embodiment]

The following will describe Fourth Embodiment of the present invention with reference to Fig. 4.

[0055]

To a parallel correlator 80 of the present embodiment, a signal 801 is supplied from an impulse radio transmitter. The parallel correlator 80 calculates respective correlation values between the supplied signal and a plurality of template trains having different phases, using a plurality of correlators, and outputs the results of the calculation

to a digital processing circuit 805. More specifically, the parallel correlator 80 includes: a plurality of correlators 804; a delay circuit 803 which generates a plurality of clocks having different phases, from a referential clock 802, and then supplies the generated clocks to the respective correlators 804; and a digital processing circuit 805 which performs processing in reaction to the receipt of the outputs from the respective correlators 804. Each of the correlators 804 is the correlators 50, 60, or 70 (cf. Figs. 5-7) for impulse radio, which have been described in one of Embodiments 1-3.

[0056]

With this arrangement, the correlations between the respective template trains having different phases and the input signal can be calculated in a parallel manner and this makes it possible to effectively utilize this calculation for operations such as the acquisition and tracking of synchronization with the input signal.[0057]

Incidentally, Japanese Laid-Open Patent Publication No. 2001-44891 (Tokukai 2001-44891; published on February 16, 2001) discloses a correlator for calculating correlation between an input signal and a code sequence which is a discrete-time signal. In contrast to this, the correlator of

the present invention is for calculating correlation between an input signal and a predetermined continuous-time signal (template train), and what is supplied to the first integrator is a continuous-time signal (signal which is not sampled). Also, the correlator of the present invention is different from the correlator of the above-mentioned document, to the extent that each of the correlators described in the respective embodiments of the present invention includes a template generator for generating a template train.

[0058]

[ADVANTAGEOUS EFFECTS]

As described, a correlator of the present invention is configured so that: a multiplier multiplies a predetermined time-series signal by the input signal; an integrator integrates an output (i) from the multiplier; a quantizer quantizes an output (ii) from the integrator; and an output (iii) from the quantizer is negatively fed back to an input of the integrator via a negative feed back path.

[0059]

In this configuration a quantization error in the quantizer output, which has been arisen in the process of

quantization, is integrated by the analog integrator, and then quantized by the quantizer again. Thus, it is possible to significantly reduce the quantization error.

[0060]

Another correlator of the present invention is characterized by comprising: a multiplier for multiplying the predetermined time-series signal by the input signal; a first integrator for integrating an output (a) from the multiplier; a sampling circuit for sampling an output (b) from the first integrator; a second integrator for integrating an output (c) from the sampling circuit; a quantizer for quantizing an output (d) from the second integrator; and a negative feedback path for negatively feeding an output (e) from the quantizer back to the second integrator.

[0061]

According to this arrangement, the quantization error negatively fed back from the quantizer to the second integrator is integrated by the second integrator, and the resulting output is requantized in the quantizer. Thus, a quantization error can be significantly decreased as in the foregoing correlator of the present invention. Further, since the first integrator requiring quick response and the

second integrator having a long holding time are provided to be independent from each other, the power consumption of the integrators can be reduced.

[0062]

According to this arrangement, in a receiver for impulse radio, it is possible to restrain the increase of the power consumption so as to decrease a quantization error (i.e. improve a S/N ratio), on the occasion of calculating the correlations between respective template trains having different phases and the input signal in a parallel manner.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

A block diagram, illustrating a substantial part of a correlator in accordance with First Embodiment of the present invention.

[Fig. 2]

A block diagram, illustrating a substantial part of a correlator in accordance with Second Embodiment of the present invention.

[Fig. 3]

A block diagram, illustrating a substantial part of a correlator in accordance with Third Embodiment of the

present invention.

[Fig. 4]

A block diagram, illustrating a substantial part of a parallel correlator in accordance with Fourth Embodiment of the present invention.

[Fig. 5]

A waveform chart, illustrating an example of a waveform of a monocycle for impulse radio.

[Fig. 6]

A waveform chart, illustrating an example of a waveform of a template for impulse radio.

[Fig. 7]

A graph, illustrating the cross-correlation between the monocycle in Fig. 1 and the template in Fig. 2.

[Fig. 8]

A waveform chart, illustrating an example of an impulse train for data transmission and an example of a template train for reception and demodulation, both being used for impulse radio.

[Fig. 9]

A block diagram, illustrating an arrangement of a radar device including a conventional correlator.

30

[REFERENCE NUMERALS]

50, 60, 70 Correlator

80 Parallel Correlator

500, 600, 700 Input Signal

501, 601, 701 Multiplier

502, 602, 702 Template Train

503, 603, 703 Template Generator

504, 604 Adder

505, 605 Analog Integrator

506, 606 Quantizer

507 Negative Feedback Path

508, 608 Digital Integrator

509, 609 Output Signal

510, 610 Clock

607 DA Converter

704 First Analog Integrator (First Integrator)

705 Sampling Switch (Switching Circuit)

706 Adder

707 Second Analog Integrator(Second Integrator)

708 Quantizer

709 Negative Feedback Path

710 Digital Integrator

711 Output Signal

712 Clock

801 Input Signal

802 Clock

803 Delay Circuit

804 Correlators

805 Digital Processing Circuit

[DOCUMENT NAME] ABSTRACT

[ABSTRACT]

[OBJECT]

To provide a correlator which is capable of improving an S/N ratio in a receiver for impulse radio, on occasion of calculating a correlation between a signal received and a template train.

[MEANS TO ACHIEVE THE OBJECT]

A multiplier 501 multiplies a received impulse train 500 by a template train502. An analog integrator505 integrates the resulting value of the multiplication. A quantizer 506 quantizes the resulting value of the integration. The quantized value is input to a digital integrator 508, and at the same time, is negatively fed back to an adder 504 provided on an input side of the analog integrator505, via a negative feedback path 507. The adder 504 adds an output from the multiplier 501 to the quantized value. In this way, a quantization error arises in the quantizer 506 is integrated in the analog integrator 505, and is re-quantized by the quantizer 506. Thus, a quantization error is reduced.

[SELECTED DRAWINGS] FIG. 1